Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 4. These sheet, which includes Fig. 4, replace the original sheet including Fig. 4.

Attachment: Replacement Sheet including Fig. 4

REMARKS

Claims 4-9 are pending in the application.

The Examiner objected to the drawings because the substrate depicted in Figure 4 is identified by the number 100, but should be the number 200 in order to be consistent with the disclosure of the instant application. Applicant has corrected this in the Replacement Sheet, including Figure 4, submitted herewith as requested by the Examiner. Proper support for the correction is found on page 9, line 25 through page 10, line 17 the specification. Accordingly, it is submitted that no new matter has been added by correcting Figure 4 as requested. Applicant believes that the submitted drawing fulfills the statutory requirements. Thus, no further correction is needed.

Rejections under 35 U.S.C. § 103

On page 3 of the Office Action, the Examiner has rejected claims 4-6, 8 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art as disclosed in figures 1-3C and their description on pages 1-7 of the instant application in view of Kanamori (6,414,346).

Applicant respectfully traverses these rejections and respectfully submits that the combination of these references should not be deemed proper under the Law, as there is no motivation, either explicator implicit, directing one of ordinary skill in the art to look to each of these references individually and thereafter pick and choose elements to ultimately arrive at the claimed liquid crystal display of the instant application. Applicant further submits that even if it were permissible to combine these three references, the claimed invention could not be considered to be obvious as certain features of the references are directed to divergent subject matter. There is no teaching for one skilled in the art to pick and choose certain elements from

any of these three references and modify certain elements to achieve what Applicant has discovered, set forth and claimed.

At the outset, there is no motivation within the reference to combine it with other knowledge in the art at the time the invention was made. Kanamori discloses a semiconductor memory that is provided with a memory cell region and a peripheral circuit region. Specifically, as depicted in Fig. 9 of Kanamori, this construction allows for the diffusion layers of the first and second select transistors Trs1 and Trs2 to be subjected to element separation by the peripheral element separating insulation films 9, thereby separating elements, such as first and second select transistors Trs1 and Trs2, to be formed in peripheral circuit region 3.

The Examiner states that it would be obvious to take the step of providing an element isolating film and isolating pattern in the outer portion of the segment select region of Kanamori with Applicant's admitted prior to arrive at Applicant's invention (Office Action, page 4). However, there is no motivation to seek an improvement in the manufacturing method of the semiconductor memory of Kanamori, which discloses an element separation insulating film which separates elements in the peripheral circuit. In particular, as noted by the Examiner, Kanamori fails to disclose an "isolating pattern at the outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from the segment select region." Thus, there is no motivation to combine the semiconductor memory that is provided with an element separation insulating film which separates elements in the peripheral circuit of Kanamori with Applicant's admitted prior art, as the combination would result in a manufacturing method of the semiconductor memory that is contrary to the disclosure of Kanamori. Kanamori teaches an

element separation insulating film which separates elements in the peripheral circuit and a method of forming the source diffusion layer and the drain diffusion layer of the semiconductor memory cells by ion implantation into the semiconductor substrate using the gate conductive layer as a mask. Therefore, this reference teaches away from the result the Examiner states would obviate the invention.

Further, Applicant submits that the manufacturing method of the semiconductor memory of Kanamori would result in a manufacturing method that lacks a drain diffusion layer in favor of a buried layer. Therefore, Kanamori fails to provide a disclosure for a buried layer and does not provide sufficient disclosure for providing an "isolating pattern at the outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from the segment select region." Applicant's invention, and specifically the combined use of an isolating film, isolating pattern and a buried layer, shows a dramatically distinct method for fabricating a mask ROM when compared with the manufacturing method disclosed in Kanamori. The isolation pattern of Applicant's invention is for separation of a buried layer from another portion of the segment select region. Moreover, because the buried layer is formed before a gate is formed, the buried layer is not a source or drain diffusion layer, as required by Kanamori.

Even if this reference was properly combinable, Kanamori alone or in combination with Applicant's admitted prior art does not disclose or render obvious Applicant's invention. Specifically, the combination of this reference and the reasons given by the Examiner for the combination do not disclose what is required by the Applicant's claims – forming an element isolating film at an outer portion of the memory cell array region and an isolating pattern at the

outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from the segment select region. This combination also does not teach or suggest a manufacturing method expressly or inherently having the claimed requirements of Applicant's method for fabricating a mask ROM. It is advantageous to provide a method for fabricating a mask ROM that has an isolating pattern at the outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from the segment select region. One advantage to using the method for fabricating a mask ROM of the present invention is that "a size of the active region is reduced to the memory cell array region of the segment, which results in improved polishing uniformity of the chemical mechanical polishing process." (Page 14, lines 4-7).

Another advantage is that "a transistor of the segment select region and a memory cell transistor of the memory cell array region are not influenced by the buried layers, thereby maintaining a homogeneous device property." (Page 13, line 23 to page 14, line 1).

The manufacturing method of Kanamori could not be used to provide a transistor of the segment select region and a memory cell transistor of the memory cell array region that are not influenced by the buried layers, thereby maintaining a homogeneous device property of Applicant's invention. Thus the manufacturing method of Kanamori is unsuitable.

Furthermore, in manufacturing a mask ROM, a buried layer is patterned in a minimum size allowable in the photolithography. Thus, it is difficult to pattern the buried layer in the boundary portion between the segment select region and the memory cell array region. In order

to resolve this problem, in a method of the present invention, an isolating pattern is formed at an outer portion of a buried layer formation region in the segment select region wherein the buried layer formation region means a region of the segment select region for a buried layer to be formed, so that a buried layer is formed in the segment select region in a minimum size with less difficulty.

In view of the aforesaid, it is respectfully submitted that claims 4 and 10 are not obvious. Applicant believes to have set forth throughout this response differences distinguishing over the individual references, as well as any combination of the references, if permissible under the Law. Absent any legally recognized motivation as discussed herein above, it is respectfully submitted that even if one were permitted to pick and choose elements from each reference in an attempt to arrive at what Applicant has claimed, one would not/could not achieve the result which is now set forth in the claims for the reasons discussed above.

Therefore, since Kanamori fails to teach or suggest forming an element isolating film at an outer portion of the memory cell array region and an isolating pattern at the outer portion of a buried layer formation region in the segment select region, the buried layer formation region defining a region for a portion of a buried layer to be formed in the segment select region, and the isolating pattern isolating the portion of buried layer from the segment select region, Applicant respectfully submits Kanamori does not render obvious any of the pending claims.

Thus, Applicant respectfully requests reconsideration and withdrawal of the § 103 rejection as to these claims and that all claims 4-10 be moved to allowance.

Conclusion

In view of the foregoing, it is submitted that, as amended, each of the remaining claims 4-9, as well as new claim 10, are now in condition for allowance and the allowance thereof is respectfully requested. The Notice of Allowance is respectfully requested to be issued.

Should any further minor objections arise or need to be attended to, the Examiner is invited to contact the undersigned attorney to discuss the matters in an effort to successfully complete the prosecution of this application.

Respectfully Submitted,

Date: 6/30/05

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